LVDSTester

User's Manual

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1 PRODUCT DESCRIPTION

1.1 General Information

LVDSTester is an automatic test equipment intended for video signal path verification during the post-production Automatic Test Procedure (ATP) in systems featuring LVDS output.
LVDSTester connects to the LVDS output on the system under test (SUT) and into a USB port on the system running the ATP routine.
LVDSTester analyzes the video frames being output to the LVDS port and signals their validity to the ATP system via the USB.
LVDSTester emulates a standard USB HID keyboard, hence no custom driver is required for ATP equipment running operating systems with native support for USB HID interface.

Additionally, LVDSTester provides an HDMI connector with DVI signalling which enables monitoring of the LVDS video on a standard HDMI/DVI monitor.

LVDSTester detects numerous problems in digital video signal path. Imagine a system being tested, which provides LVDS video output out of a native parallel RGB TTL interface. In such a system, parallel RGB is first converted to LVDS using a LVDS serializer. LVDSTester will verify digital video port functionality in both parallel RGB and LVDS subsystems.

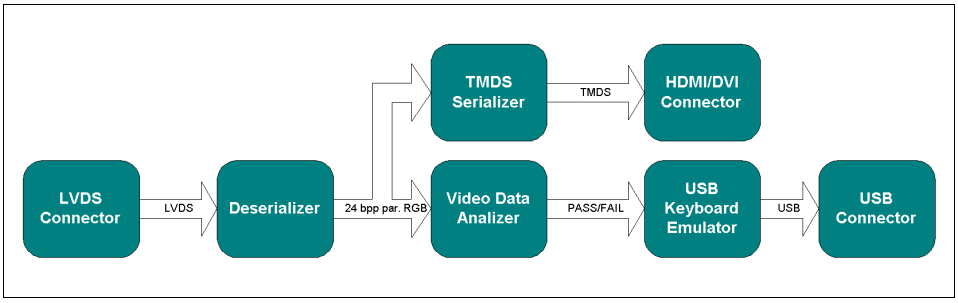
Figure 1 Explaining Entire Video Pass Checking

1.2 LVDSTester Features

- Automatic Go/No-Go LVDS Output Testing
- Direct interface to CompuLab's SBC-fitPC2i, SB-iAM, SB-iTC and other SB-xxx board series LVDS output
- Direct interface to Kontron's JILI (JUMPtec Intelligent LVDS Interface) and EPI LVDS
- Single / Dual Channel LVDS Support
- Supported resolutions: VGA up to UXGA, custom.
- 1st LVDS channel's monitoring output (DVI/HDMI)
- Plug-n-Play USB HID output (keyboard emulation)
- Stand-alone 4-Key USB Keyboard Operation
- LVDS-to-DVI (LVDS-to-HDMI) Converter Operation

1.3 Block Diagram

Figure 2 LVDSTester Block Diagram



1.4 Component Locations

1.4.1 Top Side Components

Figure 3 LVDSTester Top Side Components

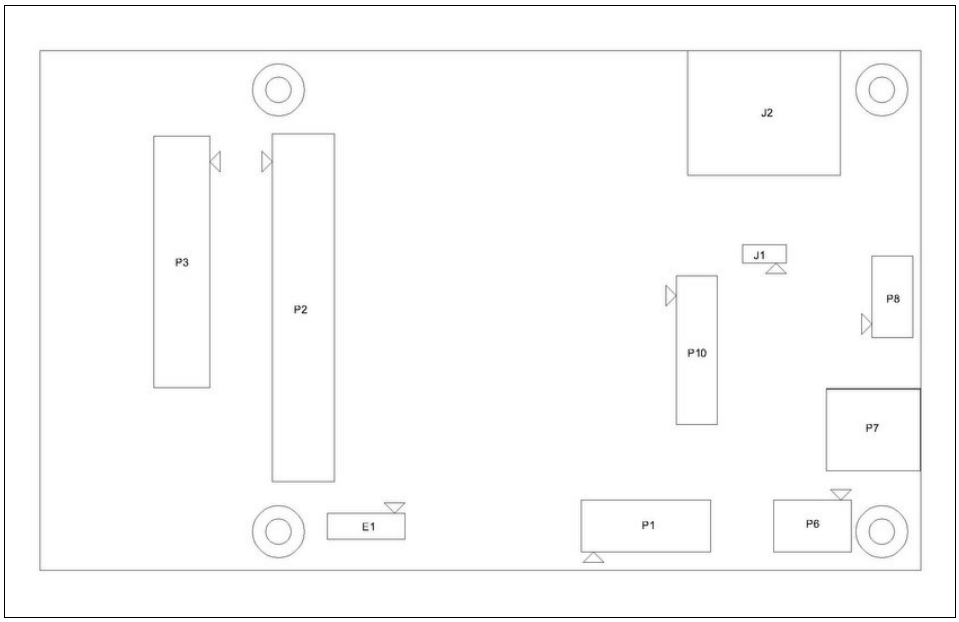


Table 1 Top Side Components Properties

Reference	Description	Note
P3	CompuLab CM-iAM, CM-iTC, CM-xAM compatible LVDS input connector	Dual cnahhel
P2	EPI LVDS connector	Dual channel
E1	Power source select jumper	
J2	DVI / HDMI monitor output	HDMI-A connector
J1	Frame analyzer mode jumper (single/dual channel)	
P8	Extra keyboard switches input (optional)	
P10	Debug header	PLD I/O
P7	USB connector to host	
P1	PLD JTAG header	
P6	HID microcontroller reflash header	

1.4.2 Bottom Side Components

Figure 4 LVDSTester Bottom Side Components

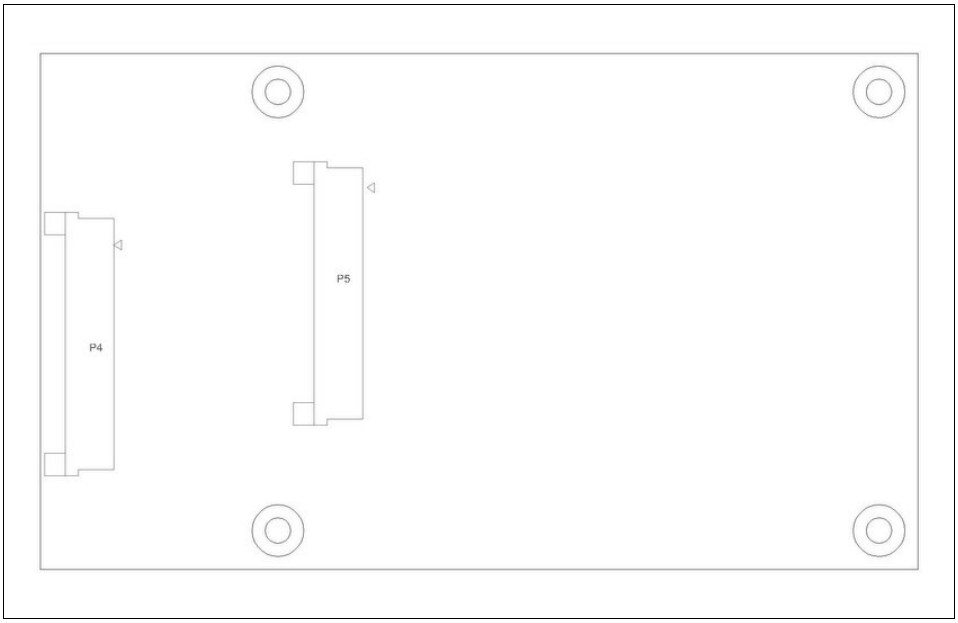


Table 2 Bottom Side Components Properties

Reference	Description	Note
P4	CompuLab SBC-fitPC2i board direct interface LVDS connector	Single cnahhel
P5	JILI-30 connector	Dual channel

1.5 Product Customization Options

On large orders a customer may customize configuration of the LVDSTester in order to reduce price.

The LVDSTester part number is of the form:

LVDSTester – L[2|3|4|5] – C[1|2] – A – D – U, where:

L – controls input LVDS connectors assembly;
C – controls number of supported LVDS channels;
A – controls assembly of analizer PLDs;
D – controls support of the DVI monitor;
U – controls support of the emulated USB keyboard.

The following section explain the L, C, A, D and U options in detail.

1.5.1 Configuration option L

Configuration option L controls the assembly of the individual LVDS input connectors.

The configuration option L is followed by one or more of the digits 2, 3, 4 and 5. These digits correspond to the connectors P2, P3, P4 or P5 and control their assembly. For example, L2, L34 and L2345 are valid options.

In product intended solely for testing the CompuLab's SBC-FITPC2i board, only the P4 connector is required, so the most appropriate configuration in this case would be L4.

1.5.2 Configuration option C

Configuration option C controls the number of the LVDS channels supported.

The configuration option C is followed by digits 1 or 2 designating number of LVDS channels receivers assembled. C1 and C2 are the only valid choices.

In product intended solely for testing the CompuLab's SBC-FITPC2i board, only the one channel is required, so the most appropriate configuration in this case would be C1.

1.5.3 Configuration option A

Configuration option A controls the assembly of the frame analizer components. If defined, leads to assembly of the analizer PLDs according to number of channels supported (option C).

Note: Configuration options combination C2 and no A is illegal.

1.5.4 Configuration option D

Configuration option D controls assembly of the DVI monitor functional module. No DVI/HDMI output will be available on the LVDSTester with this option not defined.

1.5.5 Configuration option U

Configuration option U controls assembly of the USB emulated keyboard module. Define this option when automatic test is required with pass/fail frame status transmitted over the USB to the host computer.

1.5.6 Default LVDSTester Configuration

The P/N of the stock LVDSTester is as follows:

LVDSTester – L2345 – C2 – A – D – U

1.6 Functional Description

1.6.1 Power Sources of the LVDSTester

LVDSTester may be powered from the USB VBUS or from the LVDS interface power (if any). Power rouiting is done according to the E1 jumper setting.

1.6.1.1 Powering From LVDS Interface

In order to configure LVDSTester to use the LVDS interface power, short pins 2-3 on jumper E1. This disconnects the internal 3.3V regulator and connects the LVDSTester's internal devices to the LVDS interface's power rail (3.3V).

Note: Hot-plugging the LVDS interface cable into a working system under test will induce a voltage droop on the system's 3.3V rail and most definitely lead to the system's hang or reset. Do not hot-plug the LVDSTester into a system under test when powered from LVDS interface.

1.6.1.2 Powering From USB Interface

In order to configure LVDSTester to use the USB interface power, short pins 1-2 on jumper E1. This connects the LVDSTester's internal devices to the internal 3.3V regulator and disconnects the LVDS interface's power rail (3.3V). In this mode the LVDS interface connectors may be hot-plugged into the working system to be tested.

Note: Powering from USB is not available in product with custom option U not engaged.

1.6.2 LVDS Signal Connectors

LVDSTester features 4 LVDS input connectors. Each connector is intended for directly interfacing with a different existing industry standard interface. The following sub-sections describe each interface in details.

Table 3 LVDS Connectors Manufacturer Part Numbers

Ref.	MFG and P/N	Mating Connector	Notes
P2	FCI 57202-F5217ALF	Samtec TCSD series IDC socket cable	Round conductor flat cable
P3	Hirose DF13A-30DP-1.25V	DF13-30DS-1.25C housing with DF13-2630SCF[A{04}] crimp contacts	Discrete wire
P4	CVILux CF20-401D0R0	CVILux FFCE4008T130000-300 FFC cable	FFC
P5	CVILux CF20-401D0R0	CVILux FFCE4008T130000-300 FFC cable	FFC

1.6.2.1 EPI Interface connector (P2)

EPI is an industry standard maintained by EPI consortium and described in specification document found at:: http://www.epi-standard.org/fileadmin/spec/EPI_Specification1.0.pdf P2 represents only the signal part of the EPI connector set and doesn't provide an option of powering the LVDSTester up from the LVDS interface.

Table 4 P2 Connector Signal Description

Pin	Name	Description
1	LVDS_DDCDATA	Serial configuration interface data (not in use)
2	LVDS_DDCCLK	Serial configuration interface clock (not in use)
3	N.C.	No connect
4	N.C.	No connect
5	GND	Common ground
6	LVDS_A_DN0	LVDS channel A differential data 0 negative
7	LVDS_A_DP0	LVDS channel A differential data 0 positive
8	LVDS_PPEN	Power enable. Not used.
9	LVDS_A_DN1	LVDS channel A differential data 1 negative
10	LVDS_A_DP1	LVDS channel A differential data 1 positive
11	LVDS_BLEN	Backlight Enable. Not in use.
12	LVDS_A_DP2	LVDS channel A differential data 2 negative
13	LVDS_A_DN2	LVDS channel A differential data 2 positive
14	N.C.	No connect
15	LVDS_A_CLKN	LVDS channel A differential clock negative
16	LVDS_A_CLKP	LVDS channel A differential clock positive
17	N.C.	No connect
18	LVDS_A_DP3	LVDS channel A differential data 3 negative
19	LVDS_A_DN3	LVDS channel A differential data 3 positive
20	GND	Common ground

Pin	Name	Description
21	LVDS_B_DN0	LVDS channel B differential data 0 negative
22	LVDS_B_DP0	LVDS channel B differential data 0 positive
23	GND	Common ground
24	LVDS_B_DN1	LVDS channel B differential data 1 negative
25	LVDS_B_DP1	LVDS channel B differential data 1 positive
26	GND	Common ground
27	LVDS_B_DN2	LVDS channel B differential data 2 negative
28	LVDS_B_DP2	LVDS channel B differential data 2 positive
29	GND	Common ground
30	LVDS_B_CLKP	LVDS channel B differential clock positive
31	LVDS_B_CLKN	LVDS channel B differential clock negative
32	N.C.	No connect
33	LVDS_B_DP3	LVDS channel B differential data 3 positive
34	LVDS_B_DN3	LVDS channel B differential data 3 negative

1.6.2.2 CompuLab SB-xxx Interface Connector (P3)

P3 is is a dual channel LVDS connector for directly interfacing the CompuLab's SB-iAM, SB-xAM, SB-iTC carrier board. The LVDSTester may be powered up from this interface as it has pins dedicated for input 3.3V DC power.

Note: P3 cannot be hot-plugged into a live system when LVDSTester is configured to be powered from LVDS interface because of the voltage droop on the 3.3V system rail in the system under test.

The mating connector is a discrete wire crimp contact housing, which makes the P3 connector usable for interfaces other than CompuLab's carrier boards, provided a proper custom cable.

Table 5 P3 Connector Signal Description

Pin	Name	Description
1	LVDS_BLEN	Backlight Enable. Not in use.
2	N.C.	No connect
3	VCC3_3LVDS	3.3V power input from the EUT (switched)
4	GND	Common ground
5	LVDS_A_CLKN	LVDS channel A differential clock negative
6	LVDS_A_CLKP	LVDS channel A differential clock positive
7	VCC3_3LVDS	3.3V power input from the EUT (switched)
8	GND	Common ground
9	LVDS_A_DN0	LVDS channel A differential data 0 negative
10	LVDS_A_DP0	LVDS channel A differential data 0 positive
11	LVDS_A_DN1	LVDS channel A differential data 1 negative
12	LVDS_A_DP1	LVDS channel A differential data 1 positive

Pin	Name	Description
13	LVDS_A_DN2	LVDS channel A differential data 2 negative
14	LVDS_A_DP2	LVDS channel A differential data 2 positive
15	LVDS_A_DN3	LVDS channel A differential data 3 negative
16	LVDS_A_DP3	LVDS channel A differential data 3 positive
17	LVDS_DDCDATA	Serial configuration interface data (not in use)
18	LVDS_DDCCLK	Serial configuration interface clock (not in use)
19	LVDS_B_DN0	LVDS channel B differential data 0 negative
20	LVDS_B_DP0	LVDS channel B differential data 0 positive
21	LVDS_B_DN1	LVDS channel B differential data 1 negative
22	LVDS_B_DP1	LVDS channel B differential data 1 positive
23	LVDS_B_DN2	LVDS channel B differential data 2 negative
24	LVDS_B_DP2	LVDS channel B differential data 2 positive
25	LVDS_B_DN3	LVDS channel B differential data 3 negative
26	LVDS_B_DP3	LVDS channel B differential data 3 positive
27	VCC3_3LVDS	3.3V power input from the EUT (switched)
28	GND	Common ground
29	LVDS_B_CLKN	LVDS channel B differential clock negative
30	LVDS_B_CLKP	LVDS channel B differential clock positive

1.6.2.3 CompuLab SBC-FITPC2i Interface Connector (P4)

P4 is is a single channel LVDS connector for directly interfacing the CompuLab's SBC-FITPC2i single-board computer's LVDS interface. The LVDSTester may be powered up from this interface as it has pins dedicated for input 3.3V DC power.

Note: P4 cannot be hot-plugged into a live system when LVDSTester is configured to be powered from LVDS interface because of the voltage droop on the 3.3V system rail in the system under test.

The P4 connector mates to the LVDS output on the SBC-FITPC2i by means of a FFC cable strip.

Note: The footprint of the P4 connector is mirrored as compared to the DBC-FITPC2i LVDS output connector's footprint in order to enable connection by a single-sided FFC cable.

Table 6 P4 Connector Signal Description

Pin	Name	Description
1	N.C.	No connect
2	N.C.	No connect
3	N.C.	No connect
4	N.C.	No connect
5	N.C.	No connect
6	N.C.	No connect

Pin	Name	Description
7	N.C.	No connect
8	N.C.	No connect
9	GND	Common ground
10	N.C.	No connect
11	GND	Common ground
12	LVDS_DDCDATA	Serial configuration interface data (not in use)
13	LVDS_DDCCLK	Serial configuration interface clock (not in use)
14	GND	Common ground
15	N.C.	No connect
16	N.C.	No connect
17	GND	Common ground
18	LVDS_BLEN	Backlight Enable. Not in use.
19	LVDS_PPEN	Power enable. Not used.
20	GND	Common ground
21	LVDS_A_CLKN	LVDS channel A differential clock negative
22	LVDS_A_CLKP	LVDS channel A differential clock positive
23	GND	Common ground
24	LVDS_A_DN3	LVDS channel A differential data 3 negative
25	LVDS_A_DP3	LVDS channel A differential data 3 positive
26	GND	Common ground
27	LVDS_A_DN2	LVDS channel A differential data 2 negative
28	LVDS_A_DP2	LVDS channel A differential data 2 positive
29	GND	Common ground
30	LVDS_A_DN1	LVDS channel A differential data 1 negative
31	LVDS_A_DP1	LVDS channel A differential data 1 positive
32	GND	Common ground
33	LVDS_A_DN0	LVDS channel A differential data 0 negative
34	LVDS_A_DP0	LVDS channel A differential data 0 positive
35	GND	Common ground
36	GND	Common ground
37	GND	Common ground
38	VCC3_3LVDS	3.3V power input from the EUT (switched)
39	VCC3_3LVDS	3.3V power input from the EUT (switched)
40	VCC3_3LVDS	3.3V power input from the EUT (switched)

1.6.2.4 JILI LVDS Connector (P5)

P5 is is a dual channel LVDS connector for directly interfacing the Contron's JILI LVDS interface. The LVDSTester may be powered up from this interface as it has pins dedicated for input 3.3V DC power.

Note: P5 cannot be hot-plugged into a live system when LVDSTester is configured to be powered from LVDS interface because of the voltage droop on the 3.3V system rail in the system under test.

The P5 connector mates to the device's JILI connector by means of a FFC cable strip.

Note: The footprint of the P5 connector is mirrored as compared to the JILI standard in order to enable connection by a single-sided FFC cable.

Table 7 P5 Connector Signal Description

Pin	Name	Description
1	N.C.	No connect
2	N.C.	No connect
3	N.C.	No connect
4	N.C.	No connect
5	N.C.	No connect
6	LVDS_BLEN	Backlight Enable. Not in use.
7	VCC5LVDS	5.0V power input from the EUT
8	VCC5LVDS	5.0V power input from the EUT
9	VCC5LVDS	5.0V power input from the EUT
10	VCC5LVDS	5.0V power input from the EUT
11	LVDS_B_DP3	LVDS channel B differential data 3 positive
12	LVDS_B_DN3	LVDS channel B differential data 3 negative
13	GND	Common ground
14	LVDS_B_CLKP	LVDS channel B differential clock positive
15	LVDS_B_CLKN	LVDS channel B differential clock negative
16	GND	Common ground
17	LVDS_B_DP2	LVDS channel B differential data 2 positive
18	LVDS_B_DN2	LVDS channel B differential data 2 negative
19	N.C.	No connect
20	LVDS_B_DP1	LVDS channel B differential data 1 positive
21	LVDS_B_DN1	LVDS channel B differential data 1 negative
22	LVDS_DDCCLK	Serial configuration interface clock (not in use)
23	LVDS_B_DP0	LVDS channel B differential data 0 positive
24	LVDS_B_DN0	LVDS channel B differential data 0 negative
25	LVDS_DDCDATA	Serial configuration interface data (not in use)
26	LVDS_A_DP3	LVDS channel A differential data 3 positive
27	LVDS_A_DN3	LVDS channel A differential data 3 negative
28	GND	Common ground
29	LVDS_A_CLKP	LVDS channel A differential clock positive
30	LVDS_A_CLKN	LVDS channel A differential clock negative
31	GND	Common ground

Pin	Name	Description
32	LVDS_A_DP2	LVDS channel A differential data 2 positive
33	LVDS_A_DN2	LVDS channel A differential data 2 negative
34	N.C.	No connect
35	LVDS_A_DP1	LVDS channel A differential data 1 positive
36	LVDS_A_DN1	LVDS channel A differential data 1 negative
37	LVDS_PPEN	Power enable. Not used.
38	LVDS_A_DP0	LVDS channel A differential data 0 positive
39	LVDS_A_DN0	LVDS channel A differential data 0 negative
40	N.C.	No connect

1.6.3 LVDS Receiver

LVDS receiver in each of the two channels of the LVDSTester converts the four LVDS data streams (Up to 2.38 Gbps throughput or 297.5 Megabytes/sec bandwidth) into parallel 28 bits of CMOS/TTL data (24 bits of RGB and 4 bits of Hsync, Vsync, DE and CNTL). This data is then transferred to the Frame Analizer PLD for checking pre-defined patterns.

The LVDS receiver supports pixel clocks of up to 85 MHz. Supported resolutions are: VGA, SVGA, XGA and Single Pixel SXGA for a single-channel LVDS and up to UXGA for dual-channel.

1.6.4 Frame Analizer

Frame analizer is built on a programmable logic device by Altera and depending on the firmware version may analize 18 or 24-bit data and output the pass/fail signal to a LED or to the USB keyboard emulator. Default firmware version is 18-bit.

1.6.4.1 Frame Analizer Logic

The PLD logic works as follows: each following pixel in a line is compared to the previous one and if they’re not an inversion of each other, the whole frame is marked as faulty. This implies that each line in a frame must consist of pixels of only 2 colors which are inversion of each other. Colors in different lines may differ.

Note: When in 2-channel mode, each channel carries only even or only odd pixels of each line. Thus, in this mode each n-th pixel will be compared not to the previous one, but to the pixel (n-2). Test frames for the 2-channel mode should be built accordingly

Channels mode may be chosen by jumper J1.

Table 8 Choosing Channel Mode

J1	Mode	Description
Open	Single-channel	Second channel's Frame Analizer is disabled
Short	Dual-channel	Both Frame Analizers are enabled and the PASS signal active only when both channels pass.

1.6.4.2 In-Field Upgrade

In-field upgrade of the frame analizer formware may be done using an Altera USB Blaster connected to a header P1 on LVDSTester.

Note: LVDSTested must be powered up when updating PLD firmware.

Table 9 P1 PLD Firmware Update JTAG Header

Pin	Name	Description
1	PLD_TCK	Test Clock
2	GND	Common ground
3	PLD_TDO	Test Data Output
4	VCC3_3	LVDSTester's 3.3V Power Rail
5	PLD_TMS	Test Mode Select
6	N.C.	No connect
7	N.C.	No connect
8	N.C.	No connect
9	PLD_TDI	Test Data Input
10	GND	Common ground

1.6.5 USB Keyboard Emulator

USB Keyboard Emulator is the functional module emulating a standard plug-n-play HID (Human Interface Device) recognized as a keyboard by most of the existing operating systems and not requiring any additional drivers to be installed. USB Keyboard Emulator is based on the V-USB project
http://www.obdev.at/products/vusb/index.html

and the 4-key keyboard project
http://blog.flipwork.nl/?x=entry:entry100224-003937

available under the GNU license.

1.6.5.1 USB Interface to a Host

The USB interface features a mini-USB connector P7 for connecting to the host.

Table 10 Mini-USB Connector (P7) Pinout

Pin	Name	Description
1	VBUS	5V USB power from the host
2	D-	Data negative
3	D+	Data positive
4	N.C.	Common ground
5	GND	Test Mode Select

1.6.5.2 Extra Buttons Interface

Another keyboard connector P8 is the extra buttons connector. The keyboard supports up to 4 buttons of which only one is used by the Frame Analizer to signal pass or fail state. The other 3 buttons may be used for signalling other events to the host. Connect corresponding pin to GND to emulate button press and disconnect from GND to release.

Table 11 Extra Buttons Connector (P8) Pinout

Pin	Name	Description
1	GND	Common ground
2	HID_BT1	Button 1 (doubling the Frame Analizer's PASS/FAIL signal)
3	HID_BT2	Button 2
4	HID_BT3	Button 3
5	HID_BT4	Button 4
6	GND	Common ground

1.6.5.3 HID Device Reflashing

HID Device may be reflashed in-field using the Atmel AVRISP mkll tool. Connect the AVRISP mkll to connector P6.

Table 12 HDMI Connector (J2) Pinout

Pin	Name	Description
1	HID_MISO	MISO
2	VDD3_3AVR	LVDSTester's 3.3V Power Rail
3	HID_SCK	CLOCK
4	HID_MOSI	MOSI
5	HID_RST	Reset
6	GND	Common ground

1.6.6 DVI Monitor Output

DVI Monitor functional module provides an HDMI connector and a TMDS transmitter to enable monitoring of the video signal on LVDS channel A. Any HDMI or DVI (with an appropriate adaptor) monitor supporting the input LVDS resolution may be used. Only the odd pixels will be displayed when in dual-channel mode halving the horizontal resolution.

Table 13 HDMI Connector (J2) Pinout

Pin	Name	Description
1	HDMI_D2+	Data 2 differential pair positive
2	GND	Common ground
3	HDMI_D2-	Data 2 differential pair negative
4	HDMI_D1+	Data 1 differential pair positive
5	GND	Common ground
6	HDMI_D1-	Data 1 differential pair negative
7	HDMI_D0+	Data 0 differential pair positive
8	GND	Common ground
9	HDMI_D0-	Data 0 differential pair negative
10	HDMI_CK+	Clock differential pair positive
11	GND	Common ground
12	HDMI_CK-	Clock differential pair negative
13	N.C.	No connect
14	N.C.	No connect
15	HDMI_DDC_CLK	Serial configuration interface clock (not in use)
16	HDMI_DDC_DAT	Serial configuration interface data (not in use)
17	GND	Common ground
18	+5V_DVI	+5V output to the monitor available only in U and L5
19	HPDET	Panel Detect – used to power down the transmitter

2 OPERATION MANUAL

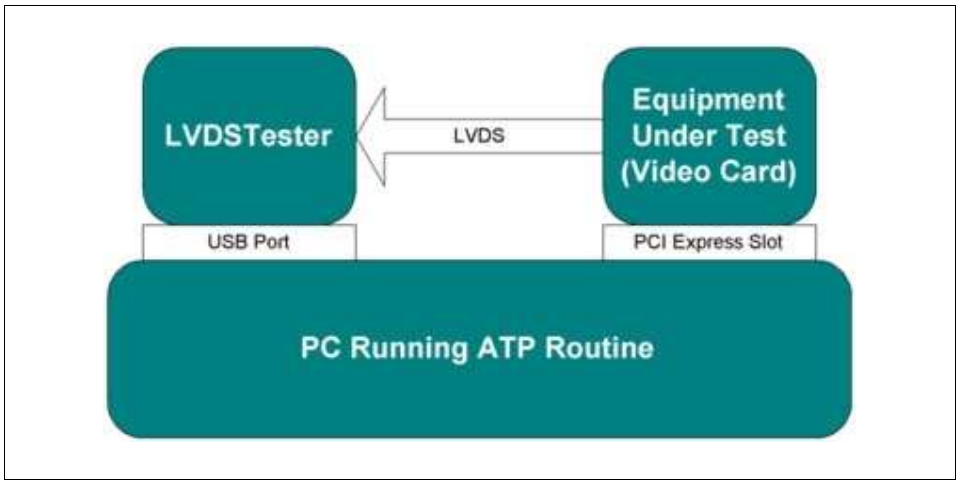
This section describes how to operate the LVDSTester in various modes, including running automated LVDS interface tests.

2.1 LVDS Automated Testing Modes

Main purpose of the LVDSTeste is using it in automatic LVDS video equipnent tests. Testing functionality of an LVDS port has never been so easy – ATP software sends test patterns and reads back virtual keyboard's scan codes reporting video frames validity.

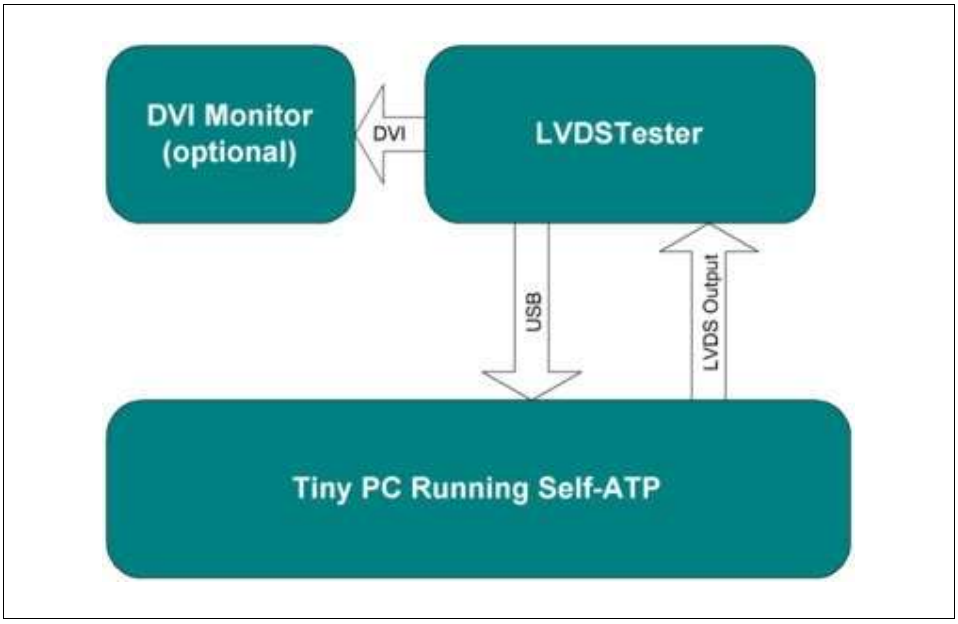
Here's an example for a PCI Express video card being tested with LVDSTester.

Figure 5 Testing Video Card LVDS Output



Another example is a tiny PC system running self-test, examines its own video output with LVDSTester without intervention of the operator.

Figure 6 Tiny PC Running LVDS Self-Test



2.1.1 Test Pattern Types

The video frame will be accepted by the LVDSTester's analizer logic as valid and PASS signal issued if each line in any individual LVDS channel's frame or half-frame consists of alternating pixels, when each following pixel in 24-bit representation is an inversion of the preceding one.

In dual-channel LVDS mode one channel transmits only the odd pixels, and the second channel – only the even pixels of the frame, while in the single-channel mode only the channel A carries all the pixels. That's why test patterns must differ for single-channel and dual-channel modes.

2.1.1.1 Single-Channel Mode Test Frames

In the single-channel mode, each line in the pattern frame must be represened by a series of interchanging pixels where each following pixel is the bit inversion of the previous one.

A frame consisting of the pixels 000000 and FFFFFF arranged in a checkerboard pattern, will be accepted as valid one in the single-mode operation.

2.1.1.2 Dual-Channel Mode Test Frames

In the dual-channel mode, each line in the individual channel's pattern frame must be represened by a series of interchanging pixels where each following pixel is the bit inversion of the previous one.

This means that in the original input frame each Nth pixel must be the inversion of the pixel N-2.

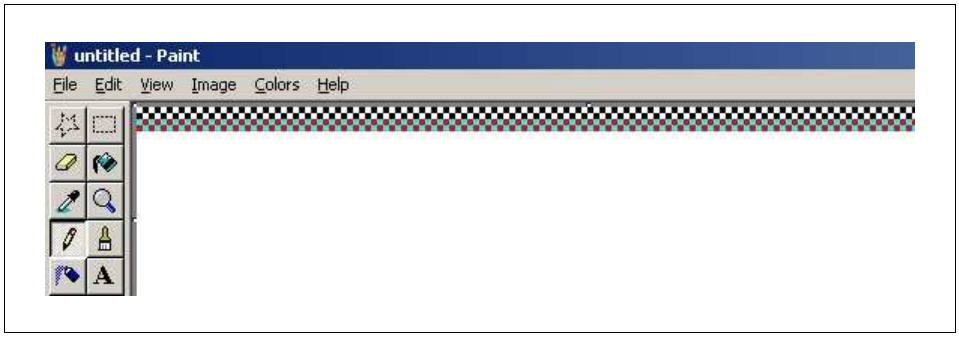
A frame consisting of the **pairs** of pixels 000000 and FFFFFF arranged in a checkerboard pattern, will be accepted as the valid one in the single-mode operation.

2.1.1.3 Generating More Test Frames

There are endless variances of possible valid frames - in each frame lines may differ one from another, the important thing is alternating inverted pixels in each line. For example, validity will be preserved if in the above examples A5A5A5 and 5A5A5A are used as the pixel colors instead of 000000 and FFFFFF.

Use your favourit graphics editor for creating more frames.

Figure 7 Process of Building a Test Frame



2.1.2 LVDS Output Requirements

For running automated LVDS output test on the System Under Test (SUT), the following conditions must be met:

- SUT should not apply any color correction schemes to the output.
- SUT should set the required video mode matching the LVDSTester capabilities.
- SUT should enable color depth (18 bpp or 24 bpp according to the LVDSTester's firmware version) in order to enable all relevant pixel bits, otherwise pattern recognition will not work.

2.1.3 Single Channel Testing

2.1.3.1 Single Channel Testing Configuration Options

The following product custom options must be present to operate LVDSTester in the Single Channel LVDS Automatic Test mode:

One or more of L2, L3, L4, L5 – input connector type;
C1 or C2 – at least one channel present;
A – Analizer present;
U – USB HID present.

Option D is optional and required if monitoring of the input LVDS data is desired.

2.1.3.2 Single Channel Test Mode Operation

Steps to operate in the Single Channel LVDS Automatic Test mode:

1. Connect mini-USB connector P7 to a host by using an appropriate cable.
2. Set the E1 jumper on pins 1-2 to set USB as a power source.
3. Leave J1 jumper open for single-channel operation.
4. Connect the LVDS cable to one of the P2, P3, P4, P5 and to the LVDS output on the system under test (SUT)
5. Configure SUT's LVDS output so the color depth is 24 bit (or 18 bit, according to the firmware version).
6. Transmit continuously any 'invalid' frames over the LVDS on the SUT. Any frame containing text information, photographs, operating system idle screen etc. will be considered as 'invalid' because it will not comply with the 'valid' frame special requirements.
7. Watch the keyboard input on the host. For example, open Notepad or pico editor and set focus in its text input window. There must be no incoming characters until frame changes to 'valid'.
8. Change LVDS output so a 'valid' frame is displayed continuously. 'p' character should now be received from the emulated keyboard. There should be no additional transmitted characters. If 'x' character is received even once while transmitting the 'valid' frame continuously, there's an error in the LVDS video path.
9. After transmitting 'valid' frame for N seconds and no 'x' character received, transmit 'invalid frame' and make sure that now 'x' received from the keyboard. Test complete.

2.1.4 Dual Channel Testing

2.1.4.1 Dual Channel Testing Configuration Options

The following product custom options must be present to operate LVDSTester in the Dual Channel LVDS Automatic Test mode:

One or more of L2, L3, L5 – input connector type;
C2 – two channels present;
A – Analizer present;
U – USB HID present.

Option D is optional and required if monitoring of the input LVDS data is desired.

2.1.4.2 Dual Channel Test Mode Operation

Steps to operate in the Dual Channel LVDS Automatic Test mode:

1. Connect mini-USB connector P7 to a host by using an appropriate cable.
2. Set the E1 jumper on pins 1-2 to set USB as a power source.
3. Close J1 jumper for dual-channel operation.
4. Connect the LVDS cable to one of the P2, P3, P5 and to the dual-channel LVDS output on the system under test (SUT)
5. Configure SUT's LVDS output so the color depth is 24 bit (or 18 bit, according to the firmware version).
6. Transmit continuously any 'invalid' frames over the LVDS on the SUT. Any frame containing text information, photographs, operating system idle screen etc. will be considered as 'invalid' because it will not comply with the 'valid' frame special requirements.
7. Watch the keyboard input on the host. For example, open Notepad or pico editor and set focus in its text input window. There must be no incoming characters until frame changes to 'valid'.
8. Change LVDS output so the 'valid' frame is displayed continuously. 'p' character should now be received from the emulated keyboard. There should be no additional transmitted characters. If 'x' character is received even once while transmitting the 'valid' frame continuously, there's an error in the LVDS video path.
9. After transmitting 'valid' frame for N seconds and no 'x' character received, transmit 'invalid frame' and make sure that now 'x' received from the keyboard. Test complete.

2.2 LVDS-to-DVI (LVDS-to-HDMI) Converter Mode

In this mode the video received on the LVDS channel A, will be converted to TMDS signalling and made available for transmitting to a DVI or HDMI display.

Every second pixel (only channel A pixels) will be displayed when in dual-channel mode, halving the horizontal resolution.

2.2.1 LVDS-to-DVI (LVDS-to-HDMI) Mode Configuration Options

The following product custom options must be present to operate LVDSTester in the LVDS-to-DVI (LVDS-to-HDMI) mode:

D – to have the DVI transmitter included;
One of L3, L4, L5 – powering from LVDS, or
L2 and U – powering from USB.

2.2.2 LVDS-to-DVI (LVDS-to-HDMI) Mode Operation

2.2.2.1 LVDS Power

1. Set the E1 jumper on pins 2-3 to power from LVDS
2. Connect the LVDS cable to one of the P3, P4, P5 and to the LVDS output on the powerd down system
3. Connect DVI or HDMI monitor to J2.
4. Power up the system providing the LVDS signal.

Now the LVDS video should be seen on the DVI/HDMI display.

2.2.2.2 USB Power

1. Connect mini-USB connector P7 to any host providing USB power by using an appropriate cable
2. Set the E1 jumper on pins 1-2 to power from USB
3. Connect the LVDS cable to one of the P3, P4, P5 and to the LVDS output
4. Connect DVI or HDMI monitor to J2.

Now the LVDS video should be seen on the DVI/HDMI display.

2.3 4-Key USB Keyboard Mode

2.3.1 4-Key USB Keyboard Mode Configuration Options

The only product custom option which should be present to operate LVDSTester in the 4-key keyboard mode, is:

U – includes the USB Keyboard Emulation functional module.

2.3.2 4-key USB Keyboard Mode Operation

Steps to operate in the 4-key keyboard mode:

1. Connect mini-USB connector P7 to a host by using an appropriate cable.
2. Set the E1 jumper on pins 1-2.
3. Connect P8 connector (Extra Buttons Connector) to your buttons.

Once the host has finished recognizing and installing the USB HID device, the key presses will be sent over the USB bus to the host as keyboard scan codes.